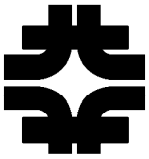

Fermi National Accelerator Laboratory

PIXEL DETECTOR PROJECT

Test Setup for FPIX Serializer Chip and SSR Chip.

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Bradley Hall

Document Revision History

Rev	Date	Author	Comments
1.0	7/24/02	B. Hall	Original
1.1	7/25/02	B. Hall	Added Hardware and PMC modifications sections.

Table of Contents

1 Introduction

This document describes the test setup, hardware requirements, and firmware description for testing a single FPIX2 serializer chip and two SSR chips.

2 Hardware

The following hardware is needed:

- PC with PTA (PCI Test Adapter) card and appropriated software to communicate with PTA card
- PMC (Programmable Mezzanine Card) loaded with firmware Rev1.0 of "FPIX2Serializer Test" firmware and with the PMC modifications as described in the following section.
- FPIX2 serializer chip mounted on preFPIX2 innerboard (contact Gabriele Chiodini for specifications/wire bonding diagrams)
- Two Serial Shift Register (SSR) chips mounted on preFPIX2 innerboard (contact Gabriele Chiodini for specifications/wire bonding diagrams)
- One 15' 25 mil pitch Hitachi cable with SAMTEC IDC terminations to connect the SSR board to the PMC SAMTEC "A" header.
- One 15' 25 mil pitch Hitachi cable with SAMTEC IDC terminations to connect the Serializer board to the PMC SAMTEC "C" header.
- One 15' 25' mil pitch Hitachi cable with a SAMTEC IDC termination on one end and two 100mil pitch terminations on other end. The two 100mil pitch terminations should be wired as shown in TBD. The end with the SAMTEC IDC connects to the PMC SAMTEC "A" header.
- Power supply: 2.5V, 3.3V, and one other channel for setting the state of some of the serializer chip parallel input word bits.

3 PMC Modifications

Termination resistors on the PMC need to be populated or unpopulated as shown in the image below:

Insert Image of PMC

4 Registers for Serializer Boards

Register 0x0000 (Read Only)	
Bit #	***Meaning***
15..0	PMC Type: 0x0000 = Undefined 0x0001 = Cable loop back test 0x0002 = FPIX0 test beam '02 0x0003 = FPIX1 test beam '02 0x0004 = preFPIX2 test beam '02 0x0005 = preFPIX2 old innerboard 0x0008 = FPIX2 Periphery BERT

Register 0x0004 (Read Only)	
Bit #	***Meaning***
7..0	Firmware Minor Revision
15..8	Firmware Major Revision

Register 0x0008 (Read/Write) - ControlA	
Bit #	***Meaning***
0	Inp0 to Serializer Board
1	Inp1 to Serializer Board
2	Inp2 to Serializer Board
3	Inp3 to Serializer Board
4	Inp4 to Serializer Board
5	Inp5 to Serializer Board
6	State of Input Lines connected to Power Supply (set to 1 if power supply voltage set to 2.5V, 0 if set to 0.0V)
7	No Connection
8	ActLines0 to Serializer Board
9	ActLines1 to Serializer Board
10	No Connection
11	ActLines3 to Serializer Board
12	Core_Talking to Serializer Board
13	No Connection
14	Clear Error Counters for Serializer Boards (Clears both the

	individual bit error counters, the word error counters (reg 0x001c), and the "Number of Words Compared" counter.
15	No Connection

Register 0x000C (Read/Write) - ControlB	
Bit #	***Meaning***
0	FPIX_RESET to Serializer Board
1	Disable Board "A" Receiver (connected to SAMTEC "C")
2	Disable Board "B" Receiver (connected to SAMTEC "B")
15..3	No Connection

Register 0x0010 (Read/Write) - ControlC	
Bit #	***Meaning***
7..0	Clk Phase Mag Adjustment (NOT IMPLEMENTED)
8	Clk Phase Mag Direction (NOT IMPLEMENTED)
14..9	No Connection
15	Clk Phase Reset (NOT IMPLEMENTED)

Register 0x0014 (Read Only)	
Bit #	***Meaning***
15..0	Received Even Bits (bits 0, 2, 4…22) from Board "A"

Register 0x0018 (Read Only)	
Bit #	***Meaning***
15..0	Received Odd Bits (bits 1, 3, 5…23) from Board "A"

Register 0x001C (Read Only)	
Bit #	***Meaning***
15..0	Number of Board "A" received 24 bit words that have at least 1 bit error.

Register 0x0324 (Read Only)	
Bit #	***Meaning***
15..0	This is the expected Even bits to receive when the serializer is set to serialize (Core_Talking = 1).

Register 0x0328 (Read Only)	
Bit #	***Meaning***
15..0	This is the expected odd bits to receive when the serializer is set to serialize (Core_Talking = 1).

Register 0x0204 (Read Only)	
Bit #	***Meaning***
15..0	This is the lower 16 bits of the 64 bit "Number of Words Compared" counter. This counter is incremented every time a received de-serialized word is compared with the expected word.

Register 0x0208 (Read Only)	
Bit #	***Meaning***
15..0	These are bits 31..16 of the 64 bit "Number of Words Compared" counter. This counter is incremented every time a received de-serialized word is compared with the expected word.

Register 0x020C (Read Only)	
Bit #	***Meaning***
15..0	These are bits 47..32 of the 64 bit "Number of Words Compared" counter. This counter is incremented every time a received de-serialized word is compared with the expected word.

Register 0x0210 (Read Only)	
Bit #	***Meaning***
15..0	These are bits 63..48 of the 64 bit "Number of Words Compared" counter. This counter is incremented every time a received de-serialized word is compared with the expected word.

Registers for Individual Bit Error Counts	
0x0020	Board “A” Bit 0 Error Count
0x0024	Board “A” Bit 1 Error Count
0x0028	Board “A” Bit 2 Error Count
0x002C	Board “A” Bit 3 Error Count
0x0030	Board “A” Bit 4 Error Count
0x0034	Board “A” Bit 5 Error Count
0x0038	Board “A” Bit 6 Error Count
0x003C	Board “A” Bit 7 Error Count
0x0100	Board “A” Bit 8 Error Count
0x0104	Board “A” Bit 9 Error Count
0x0108	Board “A” Bit 10 Error Count
0x010C	Board “A” Bit 11 Error Count
0x0110	Board “A” Bit 12 Error Count
0x0114	Board “A” Bit 13 Error Count
0x0118	Board “A” Bit 14 Error Count
0x011C	Board “A” Bit 15 Error Count
0x0120	Board “A” Bit 16 Error Count
0x0124	Board “A” Bit 17 Error Count
0x0128	Board “A” Bit 18 Error Count
0x012C	Board “A” Bit 19 Error Count
0x0130	Board “A” Bit 20 Error Count
0x0134	Board “A” Bit 21 Error Count
0x0138	Board “A” Bit 22 Error Count
0x013C	Board “A” Bit 23 Error Count

5 Registers for SSR Board

Register 0x0300 (Read/Write) - ControlC	
Bit #	***Meaning***
0	Data Input Type Select. '0' results in a pattern "10101010…" while '1' results in a pattern "1100110011001100…"
1	Clear each of the 8 SSR error counters
2	Reset the SSR receiver state machine.
15..3	No Connection

Registers for Individual Bit Error Counts	
0x0304	Errors found Chip1_Seuss
0x0308	Errors found Chip1_NAND
0x030C	Errors found Chip1_Normal
0x0310	Errors found Chip1_TripleRed
0x0314	Errors found Chip2_Seuss
0x0318	Errors found Chip2_NAND
0x031C	Errors found Chip2_Normal
0x0320	Errors found Chip2_TripleRed

6 Serializer Test Description/Procedure

The serializer test currently can test a single FPIX serializer board on the Board "A" receiver. On power-up, all registers in the PMC default to 0x0000. To start testing the serializer board use the following sequence:

Step	*Action*	*Register*	*Value*	*Description*
1	Write	0x0008	0x0800	This sets the serializer chip ActLines3 = '1'. The serializer chip is now configured in the 6-serializer mode.
2	Write	0x000C	0x0005	This Disables Board "B" (bit 2 = '1') and sets FPIX_RESET = '1' (bit 0 = '0').
3	Write	0x000C	0x0004	This keeps Board "B" disabled and deasserts FPIX_Reset. The serializer should now be sending sync words (Core_Talking still = '0').
4	Read	0x0014	0x0C01	These are the received even bits of the sync word. This should read "0x0C01". If not, there is a problem. Try repeating steps 2 and 3.
5	Read	0x0018	0x0E00	These are the received odd bits of the sync word. This should read "0x0E00". If not, there is a problem. Try repeating steps 2 and 3.
6	Write	0x0008	0x1836	This sets the serializer chip to start serializing data words. Core_Talking is set (bit 12 = '1'), ActLines3 is still set (bit 11 = '1'), and Inp1, Inp2, Inp4, and Inp5 are set (bit 1, bit 2, bit 4, and bit 5 = '1').
7	Write	0x000C	0x0005	This Disables Board "B" (bit 2 = '1') and sets FPIX_RESET = '1' (bit 0 = '0'). It is always safe to reset the board after the Inp Lines have changed
8	Write	0x000C	0x0004	This keeps Board "B" disabled and deasserts FPIX_Reset. The serializer will send sync words until the receiver acknowledges it has sync, and then start sending the serialized data word.
9	Read	0x0324	0x0A29	Read Register 0x0324 to see the expected even bits.
10	Read	0x0328	0x0618	Read Register 0x0328 to see the expected odd bits.
11	Read	0x0014	0x0A29	Read Register 0x0014 to see the actual received even bits. This should be 0x0A29, otherwise, there is a problem.
12	Read	0x0018	0x0618	Read Register 0x0018 to see the actual received odd bits. This should be 0x0618, otherwise, there is a problem.
13	Write	0x0008	0x5836	This resets the error counters (Bit 14 = '1')
14	Write	0x0008	0x1836	This disables the reset to the error counters (Bit 14 = '0'). The receiver should now be receiving and comparing the incoming data.
15	Read	0x001C	0x0000	Read register 0x001C to poll for any errors.

When an error is detected, the receiver increments the error counters, disables Core_Talking, and waits to receive sync words. Once it receives two sync words and has its sync reestablished, Core_Talking is re-asserted and the incoming de-serialized data is compared.

Read Registers 0x0324 and 0x0328 to see the expected even and odd bits, respectively.

A large 64-bit counter is incremented every time a 24 bit received data word is compared. Read this counter (it's broken into four registers) to see how many words have been compared. Multiply this by 24 to see how many bits have been compared.

FPIX2 Serializer Data Format

B. Hall 07/25/02

When Configured in 1-Serializer Mode ->	Serializer 1																			
When Configured in 6-Serializer Mode ->	Serializer 6				Serializer 5				Serializer 4				Serializer 3				Serializer 2				Serializer 1			
24 Bit Data Word Bit# ->	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EvenWord Bit# ->		11		10		9		8		7		6		5		4		3		2		1		0
OddWord Bit# ->	11		10		9		8		7		6		5		4		3		2		1		0	
Bit State ->	0	In1	In2	In3	In4	In5	0	P	P	P	P	P	0	In1	In2	In3	In4	In5	0	P	P	P	P	1
Controlling Source ->	Always '0'	Reg 0x0008 Bit 1	Reg 0x0008 Bit 2	Reg 0x0008 Bit 3	Reg 0x0008 Bit 4	Reg 0x0008 Bit 5	Always '0'	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	Always '0'	Reg 0x0008 Bit 1	Reg 0x0008 Bit 2	Reg 0x0008 Bit 3	Reg 0x0008 Bit 4	Reg 0x0008 Bit 5	Always '0'	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	External Voltage Source and Reg 0x0008 Bit 6	Word Mark Bit, Always '1'
Sync Word ->	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

7 SSR Test Description/Procedure

On power up, the SSR test starts automatically. All registers on power up default to 0x0000 resulting in the "1010101010…" pattern being sent to the SSR chips. A counter is used to generate both the CLK to the SSR chips and the Data. The CLK to the SSR chips is running at 12.5Mhz. Registers 0x0304 thru 0x0320 may have some errors in them until a reset is issued. This is because the state machine used to receive the incoming bit streams makes no attempt to account for the 120 SSR chain, but instead, only looks for the "10101010…" pattern or "110011001100…" pattern depending on the state of SSRControl (Reg 0x0300) bit 0.

Use the following sequence of events to start the SSR test:

Step	*Action*	*Register*	*Value*	*Description*

1	Write	0x0300	0x0006	This resets the error counters (bit 1 = '1'), resets the receiver state machine (bit 2 = '1') and selects the "10101010…" pattern (bit 0 = '0').
2	Write	0x0300	0x0000	This de-asserts the reset to both the error counters and receiver state machines. The receiver state machine is now checking the incoming bit streams and incrementing the error counters when an upset is found.
11	Read	0x0304	0x0000	Read register 0x0304 to poll for any errors on Chip1_Seuss. Poll registers 0x0308 to 0x0320 to check for errors from the seven other SSRs.

Note that the two SSR chips on the board…Chip1 is sensitive to the falling edge of CLK and Chip2 to the rising edge of clock (wire bonding mistake).

The receiver state machine is sensitive to the falling edge of its clock.

When the receiver state machine detects an upset, it issues an "Error Found" signal which is used to increment the error counter. It then waits until it receives a '0' on the incoming data stream and then a '1' until it restarts checking for upsets. This implies an upset the causes a long string of '1's or '0's would be counted as a single error.

8 General Comments

As a sanity check, try reading Register 0x0000 and 0x0004. These are hardwired read-only register that should read 0x0008 and 0x0100, respectively. If not, there is a problem with the PMC/PTA interface. Try the reset button on the PMC or power down and re-connect the PMC to the PTA card.

Don't use In0…its behavior is currently unknown. Leave it = to 0.

Connections are not very reliable…if in doubt, disconnect then reconnect the cables.